IN THE SPECIFICATION:

On page 9, lines 9 - 17, please replace the following paragraph:

In one embodiment, to ensure accurate delay in the delay elements, a delay line, configured in a delay lock loop, is used. The delay lock loop is automatically tuned or calibrated by adjusting parameters in the delay elements. **Figure 5** is a block diagram illustrating one embodiment for a continuous time FIR that uses tuned delay elements. Similar to the analog continuous time FIR of **Figure 3**, FIR 400 includes a plurality of the delay elements, "N" (440, 450, ~~for~~ 455, and 460). The output of each of the "N" delay elements is coupled to the input of an analog multiplier (468, 470, 472 and 474). The output of the analog multipliers 465 is input to a summing circuit 480, to generate the equalized signal output.

On page 16, lines 5 - 19, please replace the following paragraph:

As shown in **Figure 11**, the output of counter 1010, an ~~N~~ n bit value, is converted to "2^n" control lines through decoder 1020. Each control line is coupled to a switch, which in turn, couples a capacitor (1032, 1034, 1036 or 1038) to transmission line 1030. By turning on and off the switches, the output of counter 1010 effectively increases or decreases the capacitance per unit length of the transmission line segments. In one embodiment, the capacitors (1032, 1034, 1036 and 1038) are binary sized to ensure a linear delay transfer function. In one embodiment, the capacitors are implemented with metal insulator metal (MiM) capacitors. Thus, using this configuration, the delay of transmission line 1030 is increased if C_{0d} leads C_0, and is decreased if C_{0d} lags C_0. The

feedback loop closed at the phase detector ensures that the average phase of C_0 is the same as the average phase of C_{0d} with the exception of some dithering. This dithering determines the minimum capacitor size selected. In another embodiment, the delay lock loop further includes a binary to thermometer code detector to convert the N bit counter output to 2^N control lines that control 2^N identical capacitors. This alternative embodiment has the advantage of exhibiting lower transient delay variations.

On page 17, line 16 – page 18, line 9, please replace the following paragraph:

The transmission line for the continuous time FIR filter may be implemented either directly on an integrated circuit chip or off the integrated circuit chip. **Figures 12~~3~~A** and **B** illustrate embodiments for implementing the transmission lines directly on an integrated circuit chip. In one embodiment, for the on-chip implementation, the transmission line is implemented as a coplanar waveguide. The transmission line may be either differential or single ended. **Figure 13A** illustrates a cross-section of an integrated circuit that implements a differential transmission line. An integrated circuit 1200 includes a semiconductor substrate 1240. Deposed on top of the semiconductor substrate 1240 is a plurality of dielectric layers, labeled 1215 on **Figure 13A**. For this embodiment, the differential coplanar waveguide is implemented on the top metal layer with ground conductors 1210 and 1230, signal conductor 1220, and negative signal conductor 1225. In typical semiconductor processing, which utilizes copper interconnect lines, the transmission line may be implemented at the top metal layer so as to minimize loss from the semiconductor substrate. Although the conductors of the waveguide of

Figures 123A and **123B** are shown in a differential configuration, a single ended waveguide, with only a signal and ground conductors, may be used.

On page 18, line 10 – page 19, line 2, please replace the following paragraph:

In another embodiment, an on-chip transmission line may be shielded from the semiconductor substrate. **Figure 13B** illustrates a cross-section of an integrated circuit for an on-chip differential transmission line that includes shielding. As shown in **Figure 13B**, the metal layers 1250 include a metal shield 1260 at the lowest metal layer. The shield 1260 is coupled to the ground conductors of the waveguide through vias and interconnects 1265 and 1270. The shield 1260 shields the electromagnetic energy from penetrating from the waveguide into the lossy semiconductor substrate 1240. For example, for an eight (8) metal layer process with copper interconnect lines, the differential coplanar waveguide as shown in **Figure 13B**, with nine micrometer by three micrometer top layer traces separated by nine micrometers, exhibits an attenuation coefficient of approximately 0.4 Neper/cm at 20 gigahertz. This attenuation amounts to approximately 30 percent signal loss per 60 pico second delay. This amount of delay is more than 1.5*Tbit at 40 Gps, which is sufficient for certain applications. Although some signal attenuation is inevitable at such high data rates, the use of shielding reduces the loss if the substrate is lossy.

On page 19, lines 3 - 15, please replace the following paragraph:

Figure 14 illustrates one embodiment for implementing the transmission lines for the FIR filter off the integrated circuit chip. The geometry of transmission line 1310

illustrates one possible configuration for a single ended transmission line on the package of the integrated circuit. The transmission line may be implemented on the integrated circuit package or on a printed circuit board for which the FIR filter circuit is mounted. For this embodiment, the circuit includes four delays(*e.g.*, "N" equals four). As shown in **Figure ~~9~~ 14**, an integrated circuit 1300 includes a ~~D~~C_0 pin to couple the reference clock to the transmission line ~~9~~1310. Additional clocks, generated from delay of transmission line 1310, are extracted at pins ~~D~~C_1, ~~D~~C_2, and ~~D~~C_3.~~—~~ The off chip implementation of transmission line 1310 allows for much thicker ~~metalization~~ metallization than ~~metalization~~ metallization that may be achieved on-chip. In addition, attenuation may be significantly reduced if the package substrate consists of a low loss dielectric. With an external transmission line, the tuning elements may still be internal to the chip.